IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] Field of the Invention: The present invention relates generally to semiconductor fabrication. More particularly, the present invention relates to methods for making electrical interconnects from one surface of a substrate of a semiconductor component to the opposite surface of the substrate of the semiconductor component and, more particularly, to methods for fabricating a through-via in a wafer, ~~interposer~~ interposer, or other substrate.

Please replace paragraph number **[0004]** with the following rewritten paragraph:

[0004] The continued miniaturization of integrated circuits results in vias having increasingly higher aspect ratios, which term refers to the ratio of height or length to width or diameter of the via. One factor contributing to the increasingly higher aspect ratios is that the width of vias is continually getting smaller. Known processes used for filling the high-aspect-ratio vias in stacked chips, interposers and contactor boards, which are typically about fifty microns wide, have difficulty filling these vias without forming voids or keyholes in the via. Conventionally, the vias may be lined with a seed layer of a metal, such as copper, using chemical vapor deposition (CVD) or physical vapor deposition (PVD), whereafter the seed layer is coated by electroplating. As the aspect ratios of the vias get higher, it becomes more difficult to cause the plating material to line or fill the vias without vugs, ~~voids~~ voids, or keyholes therein which adversely affect the conductivity of the via.

Please replace paragraph number **[0005]** with the following rewritten paragraph:

[0005] Referring to FIG. 1, there is shown a cross-section of a substrate generally at 10. The substrate includes a via 12 that is filled using an electroplating process known in the art. The interior of the via 12 is coated with a ~~layer of~~ metal layer 14 which has been deposited using the electroplating process. Electroplating is an electrochemical process by which metal, in ionic form in solution, is deposited on a substrate immersed in a bath containing the ionic form of the

metal. A current is passed from an anode through the electroplating solution such that the metal ions are deposited on the cathode provided by a seed layer of metal of the substrate. As illustrated, a surface of the metal layer 14 is uneven and when the via 12 is filled to completion, the uneven surface may result in the formation of one or more voids in the contact mass filling the via. In other known processes, the via may be filled by an electroless plating process. In electroless plating, a seed layer may be formed by, for example, using plasma enhanced chemical vapor deposition (PECVD). The seed layer is coated by a metal layer by placing the substrate in a bath that contains metal ions in aqueous solution and a chemical reducing agent such that the metal ions are deposited on the seed layer by a chemical reduction process.

Please replace paragraph number **[0007]** with the following rewritten paragraph:

[0007] In an attempt to avoid the formation of voids and keyholes in the via, other methods have been developed to fill the vias. FIG. 3 is a cross-section of a substrate generally at 30. The substrate 30 includes a via ~~32 and is~~ 32, being filled using electroless plating as known in the art. The substrate 30 is placed in a bath for an electroless plating process, also referred to as immersion plating. As illustrated, a metal layer 34 is formed over a seed layer (not shown) on the sidewall of the via 32 by the continuous deposition of metal until the via 32 is substantially filled with the metal. However, the electroless deposition process of FIG. 3 may result in voids or depressions being present in the via 32. Further, since electroless plating is relatively slow, *i.e.*, the metal, such as nickel, is deposited at a maximum rate of approximately 20 microns per hour, the extended time to complete the deposition process may be undesirable. For instance, if the via is 70 μm wide, the deposition process would take about one and three-quarter hours to deposit about 35 μm of metal on the interior of the via 32 (70 μm/2) as the metal ~~layer~~ layer 34 grows ~~inwards towards~~ inwardly toward the center of the via to completely fill the via 32.

Please replace paragraph number **[0009]** with the following rewritten paragraph:

[0009] Accordingly, a need exists for an improved method for filling vias that is faster than known processes, does not leave voids, ~~depressions~~ depressions. or keyholes in the filled via and is cost effective to manufacture.

Please replace paragraph number **[0010]** with the following rewritten paragraph:

[0010] The present invention, in a number of embodiments, overcomes the above difficulties by providing a method for forming a conductive via in a semiconductor component and semiconductor components resulting therefrom. The methods of forming conductive vias of the present invention are faster than known processes since the conductive via is not completely filled with an electroplated or electroless plated metal. Further, the conductive vias of the present invention include an annular layer of conductive material that is substantially free of vugs, ~~voids~~ voids, and keyholes such that the conductivity of the via is not compromised.

Please replace paragraph number **[0014]** with the following rewritten paragraph:

[0014] A further exemplary embodiment of the present invention comprises a semiconductor component including a substrate having a first surface ~~and~~ and an opposing second surface and at least one conductive via extending therebetween. The at least one conductive via includes an annular conductive layer that extends from the first surface of the substrate to the second surface of the substrate. A conductive or nonconductive filler material is circumscribed by the annular conductive layer and extends from the first surface of the substrate to the opposing, second surface of the substrate.

Please replace paragraph number **[0015]** with the following rewritten paragraph:

[0015] The present invention also encompasses, in yet another embodiment, a system including a microprocessor and at least one memory device in communication with the microprocessor ~~is further disclosed~~. The at least one memory device comprises a substrate having a first surface and an opposing, second surface and at least one conductive via extending

therebetween. The at least one conductive via includes an annular layer of conductive material extending from the first surface of the substrate to the opposing, second surface of the substrate. A conductive or nonconductive filler material is circumscribed by the annular layer of the conductive material and extends from the first surface of the substrate to the opposing, second surface of the substrate. The memory device also includes at least one bond pad overlying the at least one conductive via.

Please replace paragraph number **[0019]** with the following rewritten paragraph:

[0019] FIG. 3 depicts a cross-section of a substrate having a via filled using an electroless plating process as known in the art;

Please replace paragraph number **[0033]** with the following rewritten paragraph:

[0033] As shown in FIG. 5B, a seed layer 128 of a conductive material is deposited over the first surface 114 and second surface 116 of the substrate 112, and the inner surface 120 of the via 118, wherein the seed layer 128 coats the insulative layer 126 (shown in FIG. 5A). For ease of illustration, the insulative layer 126 of drawing FIG. 5A is omitted from FIG. 5B and other subsequent drawings. In the illustrated embodiment, the seed layer 128 comprises titanium nitride (TiN) and is deposited by CVD. Other materials that may be used as the seed layer 128 include, without limitation, titanium (Ti), silicon nitride (Si_3N_4), a polysilicon, tantalum nitride (TaN), and copper. Other deposition processes that may be used to deposit the seed layer 128 include PVD, atomic layer deposition (ALD), PECVD, vacuum ~~evaporation~~ evaporation, and sputtering. It will be apparent that the selection of the type of material and deposition process utilized to deposit the seed layer 128 will vary depending on the type of material used to form the electrical interconnect through the via 118.

Please replace paragraph number **[0045]** with the following rewritten paragraph:

[0045] The semiconductor component 200 includes a blind via 218 that partially penetrates the substrate 212 and substantially extends through the substrate 212 from the first

surface 214 and wherein a bottom 213 of the blind via 218 terminates short of the second surface 216 of the substrate 212. The blind via 218 may be formed in the substrate 212 using a laser ablation process or in any other manner as the via 118 was formed in the substrate 112 as described herein with reference to FIG. 5A. The blind via 218 is circumscribed by an inner surface or sidewall 220 of the substrate 212. The portion of the substrate ~~112~~ 212 that circumscribes an uppermost edge 222 of the blind via 218 is illustrated in broken lines which, for ease of illustration, is omitted from subsequent drawings.

Please replace paragraph number **[0056]** with the following rewritten paragraph:

[0056] Another exemplary embodiment of acts in the methods of the present invention is depicted in FIGS. 7A and 7B. A semiconductor component is shown generally at 200'. The semiconductor component 200' includes a substrate 212 having a first surface 214 and an opposing, second surface 216. A barrier layer 203 is formed on the first surface 214 of the substrate 212. The barrier layer 203 comprises a material that prevents a seed layer 228 from being deposited thereon. The barrier layer 203 may comprise an oxide- or a nitride-containing material such as silicon dioxide or silicon nitride. A blind via 218 is formed through the barrier layer 203 and in the substrate 212. A seed layer 228 and conductive layer 230 are formed in the blind via 218, whereafter the remaining ~~space~~ opening 234 of the blind via 218 is filled with the filler material as previously discussed herein. The fabrication of the conductive blind via 218 may be completed as previously described.

Please replace paragraph number **[0059]** with the following rewritten paragraph:

[0059] As noted, the substrate 312 of the semiconductor component 300 may be designed and fabricated as an interposer for connecting various semiconductor components, as a semiconductor test substrate (contactor board) or as a carrier substrate forming higher-level packaging to which semiconductor chips may be connected. If configured as a semiconductor device with active ~~circuitry~~ circuitry, the bond pads 338 or contact pads 342 of the semiconductor component 300 may be arranged in a pattern that corresponds to that of terminal

pads on a test or carrier substrate. If used as an interposer or contactor board, bond pads 338 or contact pads 342 may be arranged in a pattern on one side of substrate 312 to correspond to terminal pads of a test or carrier substrate and on the other side to correspond to bond pad or other I/O locations on a semiconductor device to be contacted.

Please replace paragraph number **[0061]** with the following rewritten paragraph:

[0061] The above-illustrated embodiments of the present invention disclose electrical interconnects in the form of through-vias that may be fabricated using low-cost materials, ~~require~~ requiring simple ~~methods~~ methods, and ~~result~~ resulting in robust electrical interconnects that are substantially free of voids and keyholes. Although the present invention has been depicted and described with respect to various exemplary embodiments, various additions, deletions and modifications are contemplated from the scope or essential characteristics of the present invention. Further, while described in the context of semiconductor devices or interposers, the invention has utility for forming electrical interconnects in any device or component fabricated with semiconductor components. The scope of the invention is, thus, indicated by the appended claims rather than the foregoing description. All changes that come within the meaning and range of equivalency of the claims are to be embraced within their scope.